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Substitute for form 1449A/PTO				<i>Complete if Known</i>	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Application Number	
				Filing Date	
				First Named Inventor	Andrews
				Group Art Unit	
				Examiner Name	
Sheet	1	of	2	Attorney Docket Number	MS1-1839US

Examiner Signature		Date Considered	4-1-05
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Substitute for form 1449B/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Application Number	
Sheet	2	of	2	Filing Date	
				First Named Inventor	Andrews
				Group Art Unit	
				Examiner Name	
				Attorney Docket Number	MS1-1839US

NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.			T ²
P.WK		YAMACHI, et al.; "The Technique for Object and Collision Detection by Z-buffer"; Department of Computer and Information Engineering; Nippon Institute of Technology; Vol. 43; No. 6; June 2002; pp. 1899-1911. <i>Abstract only</i>			
		WHITE, et al.; "The Tayra 3-D Graphics Raster Processor"; Comput. & Graphics, Vol. 21; No. 2; pp. 129-142; 1997			
		BRESENHAM; "Teaching the graphics processing pipeline: cosmetic and geometric attribute implications"; Computers & Graphics 25 (2001) 343-349; 7pages:			
		DOCTOR, et al; "Using raster scan in color graphics"; Mini-Micro Systems; December 1981; pp. 101-108			
		WHITTED; "Hardware Enhanced 3-D Raster Display System"; CMCCS '81/ACCHO '81; pp. 349-356			
		FUCHS et al; "Pixel-Planes: A VLSI-Oriented Design For 3-D Raster Graphics"; CMCCS '81/ACCHO'81; pp. 343-347			
		PARKE; "Simulation and Expected Performance Analysis of Multiple Processor Z-Buffer Systems"; 1980 ACM 0-89791-021-4/80/0700-0048; pp. 48-56			
↓		CHEN et al.; "Reduce the Memory Bandwidth of 3D Graphics Hardware With a Novel Rasterizer"; Journal of Circuits, Systems, and Computers, Vol. 11; No. 4; (2002) pp. 377-391			

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